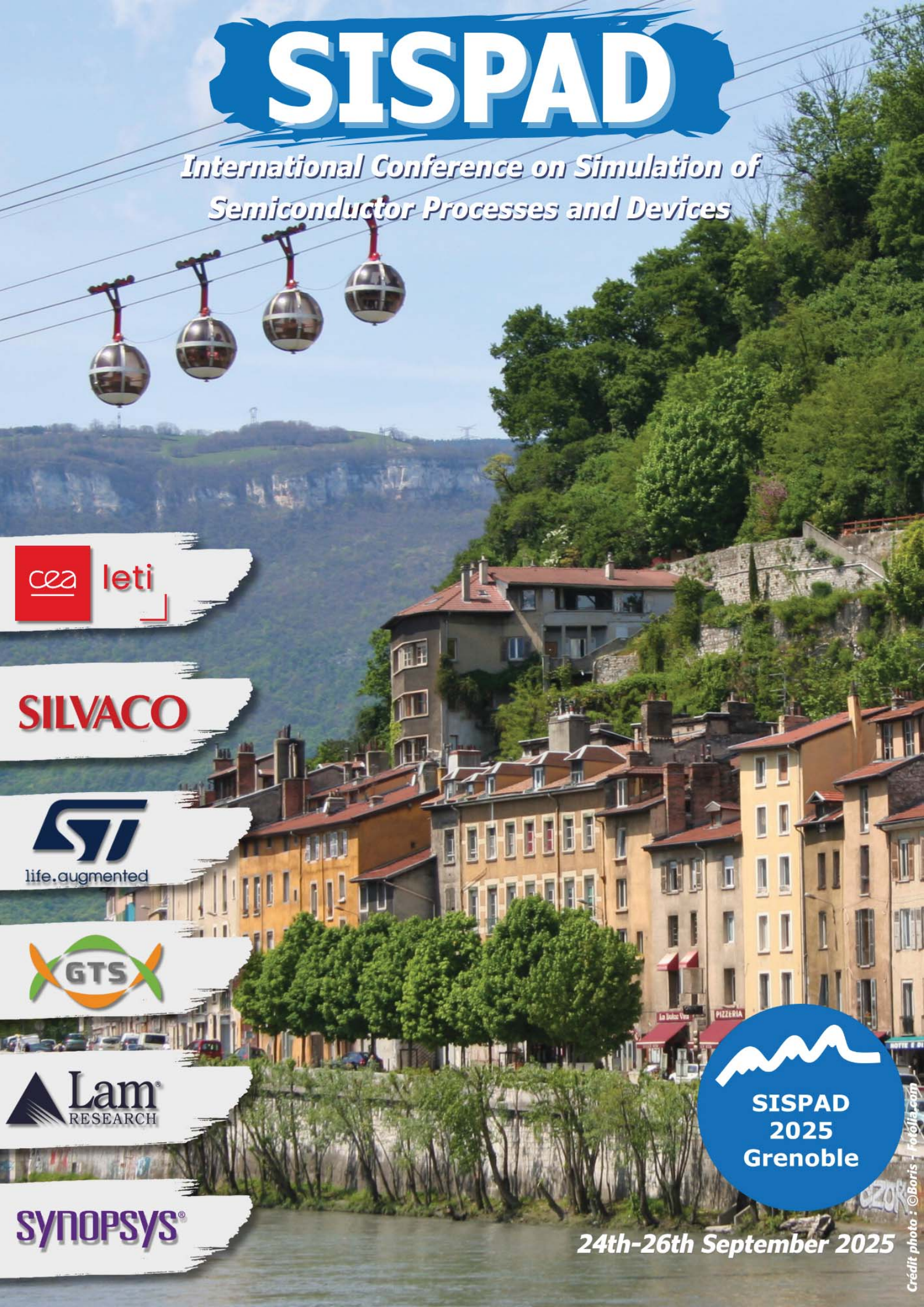
SISPAD

International Conference on Simulation of Semiconductor Processes and Devices



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SISPAD 2025 Grenoble

24th-26th September 2025

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Contents

Welcome

Dear Colleagues,

We are thrilled to invite you to the 30th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), which will take place in Grenoble, France, from September 24th to 26th, 2025. Since its establishment in 1996, SISPAD has become a premier platform for showcasing and discussing the latest advancements and innovations in semiconductor process, device, and circuit simulations, as well as their applications to advanced devices.

The 30th edition of SISPAD promises an exceptional program featuring 19 sessions, including 3 plenary talks, 8 invited talks, 59 contributed talks, and 29 poster presentations. The research presented will cover a wide range of topics in semiconductor and advanced modeling, such as process/device modeling for established logic, memory, and power devices, 2-D materials, ferroelectric modeling, sensors and optoelectronics, machine learning and AI-based modeling, chip-level and packaging modeling, and quantum computing. Additionally, a workshop program is scheduled for September 23rd, 2025, focusing on the themes "Advanced topic in Microelectronic Simulations" , and “Emerging Artificial Intelligence , neural network and differentiable programing”.

The success of this year’s technical program is a testament to the hard work and dedication of the Technical Program Committee and the conference organizing committee, chaired by Sebastien Martinie and Bruce Rae. We extend our heartfelt thanks to the authors for their high-quality contributions and to the steering committee members for their invaluable guidance and support. We hope you will find the presentations and discussions both enlightening and inspiring, and that you will take advantage of the numerous networking opportunities with fellow colleagues and subject matter experts. We warmly welcome all speakers and attendees to SISPAD 2025 and look forward to a memorable and productive conference.

Best regards,

The SISPAD 2025 Organizing Committee

J-C. Barbé (CEA-Leti, chair)

D. Rideau (STMicroelectronics, co-chair);

SISPAD 2025

International Conference on Simulation of Semiconductor Processes and Devices

September 24 – 26, 2025 – Grenoble, France

The conference will be held in person at Maison MINATEC Congress Center located in MINATEC Campus in Grenoble.

The International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) serves as a global platform for presenting cutting-edge research and advancements in process and device simulation. As one of the longest-standing conferences dedicated to technology computer-aided design (TCAD) and the advanced modeling of novel semiconductor devices and nano-electronic structures, SISPAD continues to be a leading forum in the field.

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Venue

General information

The workshop will be held at Maison MINATEC Congress Center located in MINATEC Campus in Grenoble, France on September, 24–26, 2025.

Nestled at the foot of the majestic French Alps, Grenoble is a city that seamlessly blends historical charm, scientific excellence, and a high quality of life. As the capital of the Isère department and a crossroads between France, Switzerland, and Italy, Grenoble appeals to both nature lovers and enthusiasts of culture and technology.

Surrounded by three mountain ranges — the Chartreuse, Vercors, and Belledonne — the city offers breathtaking views in every direction. Often referred to as the “Capital of the Alps,” Grenoble lives in harmony with the seasons: hiking and outdoor activities in summer, and winter sports just a short drive away when the snow falls. One of the city’s most iconic attractions is the cable car — affectionately known as "Les Bulles" (The Bubbles) — which whisks visitors up to the Bastille fort for sweeping panoramic views over the city and surrounding peaks.

Photo credit: utopikphoto

Yet Grenoble is more than just a gateway to nature. It is also a hub of innovation and forward-thinking. Renowned for its universities and research centers, the city is home to prestigious institutions such as the CEA, the European Synchrotron Radiation Facility, and numerous startups and tech clusters. This blend of tradition and modernity is visible throughout the city: the cobbled streets and historic architecture of the old town coexist with the sleek, contemporary design of the scientific district on the Presqu’île. Grenoble is a major, world-wide scientific center. The technical expertise and the synergy between university, research and industry contribute to its successful image.

MINATEC campus is one of the examples illustrating the vitality and the diversity of microelectronics activity in Grenoble area. It is one of the few places worldwide to bring together the human, corporate and material resources needed to rise to the challenge of further miniaturization.

As a City of Art and History, Grenoble offers a wealth of cultural attractions. The Musée de Grenoble

is one of the finest art museums in France outside Paris, featuring a diverse collection that spans from classical to modern and contemporary works. The Musée Dauphinois, housed in a former convent, provides fascinating insights into local Alpine traditions and regional history.

Grenoble is also known for its lively, welcoming atmosphere. Its bustling markets, restaurants showcasing local specialties — such as ravioles or the creamy gratin dauphinois — cultural festivals, and vibrant student population make it a city full of energy and warmth.

Photo credit: Pierre Jayet

Access

By Car

Grenoble is easily accessible by car from several major cities:

- **From Geneva or Chambéry (A41 motorway):** Take the Rocade Sud ring road and follow signs marked "Lyon par l'autoroute." Exit the motorway at the Europole turn-off and follow signs to MINATEC.
- **From Lyon (A48 motorway):** Exit the motorway at the Europole turn-off and follow signs to MINATEC.

Distances from Grenoble:

Lyon:	100 km
Geneva:	145 km
Torino:	240 km
Nice:	330 km
Paris:	570 km
Barcelona:	625 km

By Plane

Grenoble is served by several international airports, each offering different options for reaching the city:

Lyon-St. Exupèry Airport

www.lyonaeroports.com/en
Approximately 1 hour drive by car. Taxi fares are around €140 (Tel: 0826 800 826). An airport shuttle bus operated by FAURE VERCORS runs hourly between 4:00 am and 12:30 pm (Tel: 0825 825 536, cost: €0.118/min). More info at www.faurevercors.fr.

Geneva-Cointrin Airport

www.gva.ch/en
Approximately 1.5 to 2 hours drive. Taxi fares around €220 (Tel: +41 22 798 20 00). Airport shuttle: www.flixbus.fr

Paris Airports

www.parisaeroport.fr/en
Take the TGV train directly from Paris to Grenoble railway station. From the airport, take the RER subway to Gare de Lyon station and transfer to the TGV.

Grenoble Isère Airport

www.grenoble-airport.com/en
About 35 minutes drive from Grenoble (Tel: +33 (0)4 76 65 55 32).

By Train

Grenoble is well connected by high-speed rail:

- The TGV line between Grenoble and Paris takes approximately 3 hours.
- There are 7 daily trains, with additional services from cities like Lille and Nantes.
- Grenoble Gare SNCF contact: +33 8 92 35 35 35 (registration).
- For schedules and bookings, visit www.sncf-connect.com/en-en.

Specific Information

Entry Requirements and Visas

For up-to-date information on entry requirements for France, please consult the official government resources:

- Entry of a foreigner in France: service-public.fr
- Visa application form: france-visas.gouv.fr
- Business travel visa details: france-visas.gouv.fr/business-travel

Conference Language and Time Zone

The official language of the conference is English, which will be used for all presentations and printed materials.

In September, Grenoble observes Coordinated Universal Time (UTC) + 2 hours.

Climate

September in Grenoble features mild, temperate weather:

- Average high temperature: 22°C
- Average low temperature: 10°C

Rain showers are possible; we recommend bringing light clothing and a raincoat.

Currency and Tipping

The official currency is the Euro (€). Exchange rates fluctuate daily; for current rates, visit: www.exchangerate.com.

France applies a Value Added Tax (T.V.A) of 20.0% included in prices. Visitors may claim this tax back on qualifying purchases when leaving the country.

Tipping is generally included in the service charge at restaurants, hotels, and taxis, so additional tipping is not customary.

Electricity

Standard European 2-pin round sockets are used, supplying 220 Volts at 50 Hz frequency. Visitors should bring appropriate plug adapters if needed.

Presentation of speakers

Plenary speakers

Emmanuel Leroux

Emmanuel Leroux is leading the EDA (Electronic Design Automation) strategy for the Simulation Brand (SIMULIA) at Dassault Systemes. His job, with his Team, is to propose RD, Partnership to meet a 3Y/6Ytarget for Multi-domain / Multi-scale MODeling and SIMulation (MODSIM) in Electronics involving also manufacturing process simulation. His responsibility includes also more tactical steps and guidance of Go-To-Market and Marketing for the simulation of Semiconductors and PCB (Printed Circuit Boards). Emmanuel received his Ph.D in Electronics in 1998 at University of Lille in France working together with Politecnico di Torino in Italy. In 1994, he joined High Design Technology (Torino) as a PCB Signal Integrity Applications Engineer. In 2020 he joined Computer Simulation Technology (CST), first as Application Engineer (Darmstadt, Germany) and then opening the CST office in Italy. From 2005 he was CST Country Manager for the Southern East Mediterranean area. After the acquisition of CST by Dassault Systèmes in 2016, he led the multi-domain simulation technical/sales Team in that same area. In 2021, he joined Dassault Systèmes SOLIDWORKS Team with the responsibility to launch the Electromagnetic simulation business within SOLIDWORKS resellers at Worldwide level. With his new position Emmanuel has the ambition to plug in EDA MODSIM into a PLM/MBSE/Generative AI framework.

Title: Virtual Twins for Semiconductor Design and Manufacturing Processes

Abstract: In the semiconductor industry, precision in design, and control in manufacturing are among critical points for innovation and yield. Virtual Twins offer a powerful approach by integrating multi-physics, multi-scale modeling and simulations (MODSIM) across key design and manufacturing steps. This article highlights some of Dassault Systèmes solutions' capabilities, including 3D electromagnetic layout simulation to evaluate circuit performance, plasma simulations for etching and deposition to optimize material processing during fabrication, deformation analysis during wafer cleaning, and chemical mechanical planarization simulations to minimize defects and ensure surface uniformity. Powered by the 3DEXPERIENCE® platform, these solutions provide an end-to-end virtual environment to reduce variability, improve yield and performance, while uniquely close the designmanufacturing loop by enabling continuous, data-driven feedback and rapid process optimization.

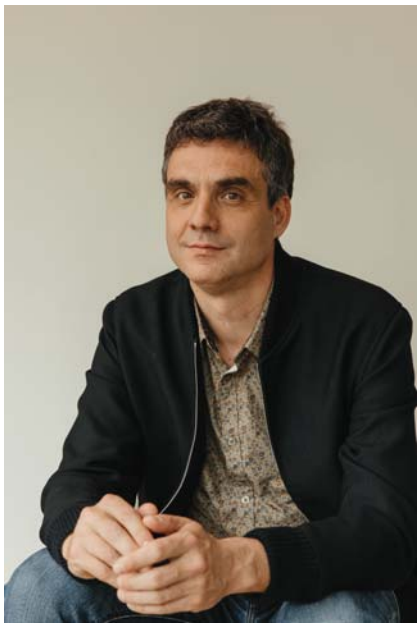
Elisa Vianello

Elisa Vianello is a senior scientist at CEA-Leti. Her primary research interests revolve around the development of new technologies for bio-inspired neuromorphic computing, with a particular focus on resistive switching memory devices. In 2022, Elisa was awarded an ERC Consolidator Grant for her research on "Heterogeneous integration of imprecise memory devices to enable learning from a very small volume of noisy data". She has been a member of the VLSI Technical Program Committee (TPC) since 2023. Elisa obtained her Ph.D. in Electrical Engineering jointly from the Università degli Studi di Udine (Italy) and the Grenoble Institute of Technology (INPG, France) in 2010.

Title: Resistive memories: multifaced impact on neuromorphic computing

Abstract: Demand for energy-efficient AI has driven significant interest in Compute-In-Memory (CIM) architectures based on memristor devices, which reduce energy consumption and latency by minimizing data movement. However, practical deployment remains limited by device variability and limited precision. This work explores how such stochastic properties can be harnessed — rather than suppressed — through Bayesian CIM, where memristors naturally encode probability distributions for uncertainty-aware inference. We review recent advances toward enabling on-chip learning at the edge, including hybrid synapses that decouple inference from learning. In addition, we examine algorithmic frameworks such as meta-learning, which retains global training in the cloud while supporting efficient edge adaptation. We also discuss biologically inspired mechanisms to mitigate catastrophic forgetting. Finally, we highlight the role of heterogeneous integration and 3D architectures as key enablers of future scalable, neuromorphic systems.

Tristan Meunier



Tristan Meunier is the Chief Technology Officer (CTO) at Quobly, where his job is to make sure that the company's future quantum computer works. An accomplished experimental physicist internationally-known for his groundbreaking research on the coherent transport and manipulation of spins in quantum dot arrays, Tristan did his PhD at the Laboratoire Kastler Brossel (LKB) of the École Normale Supérieure (ENS) in Paris under the tutelage of Nobel Laureate Serge Haroche followed by a postdoctoral fellowship at TU Delft—a pioneering center for experimental research on spin qubits. This postdoc shaped Tristan's vision of science as a means of advancing humanity. Following a European Research Council (ERC) Starting Grant for his research on the coherent control of individual electron spins in semiconductor nanostructures and, later, a Synergy Grant with Maud Vinet and Silvano de Franceschi, Tristan led Grenoble's quantum spin qubit community at the French National Center for Scientific Research (CNRS) before joining Quobly as CTO full-time. He hopes to see quantum computing make a real difference in biotechnology and drug discovery.

Title: Transport characterization and quantum dot coupling in commercial 22FDX®

Abstract: Different groups worldwide have been working with the GlobalFoundriesTM 22nm platform (22FDX®) with the hopes of industrializing the fabrication of Si spin qubits. To guide this effort, we have performed a systematic study of six of the foundry's processes of reference (POR). Using effective mobility as a figure of merit, we study the impact of gate stack, channel type and back bias as a function of temperature. This screening process selected qubit devices that allowed us to couple quantum dots along both the length and width of the Si channel. Simulations provide insights into potential technology optimizations and the advantages of leveraging forward body bias within an FDSOI qubit platform.

Half-Plenary speakers

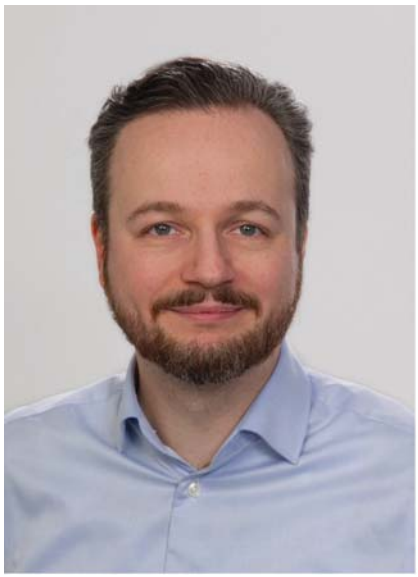
Eric Guichard

Eric Guichard, Ph.D., has over 30 years of experience in the semiconductor industry. Dr. Guichard serves as Senior Vice President and General Manager of Silvaco's TCAD division since November 2012 and served as Vice President of Applications from July 2008 to November 2012. From September 1995 to July 2008, Dr. Guichard served in various roles with Silvaco SA, formerly known as Silvaco Data Systems, one of the wholly owned subsidiaries of Silvaco Inc., including as a General Manager and Applications Engineer. Eric Guichard received a M.S. in materials science and a Ph.D. in semiconductor physics from Institute National Polytechnique de Grenoble, France.

Title: Driving Four Decades of TCAD Innovation: From Physical Simulation to AI-Powered Digital Twins

Abstract: Fueled by the highly paced electronics industry, today's cutting-edge device designs regularly make use of intricately shaped, multi-material, and ultra-confined 3D heterostructures and exploit strain, size, and quantum effects. These translate to progressively more complex physical modeling and simulation efforts, which is further intensified when optimization workflows are needed, such as Design Technology Co-Optimization (DTCO). All of this puts further pressure on industrial development cycles and workforce demands. The goal must be the abstraction of complexity to allow for a wider user base to get fast responding access to the knowledge TCAD provides. This is provided by Fab Technology Co-OptimizationTM (FTCOTM) which allows for the AI-driven training of a Digital Twin (DT) model based on comprehensive process-to-circuit level TCAD simulation data complemented by Fab data. The DT model provides instantaneous feedback to non-TCAD experts who need to understand correlations between individual process parameters and specific device and/or circuit characteristics. This allows for on-the-spot decision making in the Fabs, aiding in optimizing process and design decisions, accelerating development cycles, and reducing workforce demands.

Zlatan Stanojevic

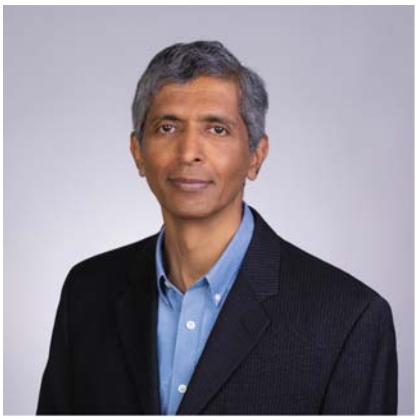


Zlatan Stanojević is the Chief Technology Officer (CTO) of Global TCAD Solutions (GTS), an independent European TCAD software vendor, where he supervises the company's RD activities. His research interests include process and device TCAD, semi-classical and quantum modeling of carrier transport effects in low-dimensional structures, Design-Technology Co-Optimization, as well as simulator design and numerical algorithms. He is the lead designer of the commercially successful GTS Nano Device Simulator (NDS), a Subband-Boltzmann-Transport-based device simulator. He has also co-supervised the development of the parasitics extraction engine PEX, part of GTS Cell Designer, and the GTS ProSim process simulation software.
Zlatan studied Microelectronics at the Vienna University of Technology where he received his MSc and PhD degrees in 2009 and 2016, respectively. He was member of the IEDM Modeling and Simulation subcommittee in 2021 and 2022 and its chair in 2023, and has been part of the ESSERC Track 3 TPC since 2019, which he is chairing in 2025.

Title: Is there anything left to do in TCAD?

Abstract: Over the past decade, the development of commercial Technology Computer-Aided Design (TCAD) software has followed an evolutionary rather than revolutionary path. Alongside established continuum and particle-based approaches in both process and device simulation, advanced carrier transport models – such as deterministic bulk and subband Boltzmann Transport Equation (BTE) solvers and Non-Equilibrium Green's Functions (NEGF) – have been incorporated into the TCAD toolkit for single-device simulation. At the system level, the field of Design-Technology Co-Optimization (DTCO) has expanded to encompass variability, reliability, and the extension of TCAD methodologies from devices to circuits. However, most of these innovations were introduced over a decade ago, prompting the question: What remains to be developed in TCAD? This talk addresses this question by analyzing current limitations and potential future directions in TCAD across three key dimensions: (1) Fidelity, (2) Integration, and (3) Efficiency – each with particular relevance in commercial and industrial contexts. We examine ongoing challenges in classical TCAD, advanced transport modeling, and DTCO flows, and propose remedies supported by specific tools and examples. Among these remedies, we include various methodologies related to artificial intelligence, machine learning, and hardware accelerators, particularly within the Efficiency dimension.

Srinivas Raghvendra



Srinivas Raghvendra is Vice President of Engineering and leads the TCAD, Mask Solutions and Smart Manufacturing group at Synopsys. His group works on software solutions that help optimize the technology development and manufacturing process. Previously he has held senior RD positions in the design implementation groups at Synopsys. His worked has spanned logic synthesis, physical design, low power synthesis, OPC/Lithography, TCAD, and Smart Manufacturing technologies. Srini has been involved with the IC design and EDA industry for over 30 years. He is the co-author of 2 patents in logic synthesis. He has delivered several invited talks at conferences, and participated in many industry panels.
Srini is a graduate of the Stanford Executive Program of the Graduate School of Business at Stanford University and has a BSEE, and a MS in Computer Science.

Title: Advances in Power Electronics Design Fueled by Hyperconvergence

Abstract: Power electronics is at an inflection point, with innovative power transistor design being introduced to serve a variety of applications like fast chargers for consumer devices, EV traction inverters and on-board chargers, LIDAR, data center power supplies, and integrated voltage regulators. While Si power transistors still comprise most of the market, SiC and GaN power transistors are increasingly being adopted in applications where the higher power capability of SiC and faster switching frequency of GaN offers compelling system benefits, while ultra-wide bandgap (UWBG) materials such as Ga2O3, AlN and diamond are being explored to offer further system level benefits. Power transistor design requires co-design of the active area unit cells, edge terminations and in-chip gate interconnects. Recent advances in meshing techniques, GPU acceleration of numerical algorithms, and physics models for Si, WBG and UWBG materials enable 3D TCAD design of edge terminations and electro-thermal layout optimization to minimize in-chip current and temperature non-uniformities. Traditionally, power transistor design has been addressed sequentially with multiple trial-and-error iterations. A hyperconvergence of design tools covering a wide range from ab-initio material engineering to 3D TCAD, electro-thermal analysis, and layout optimization of the power transistor is being introduced to address all these critical design aspects in an automated way.

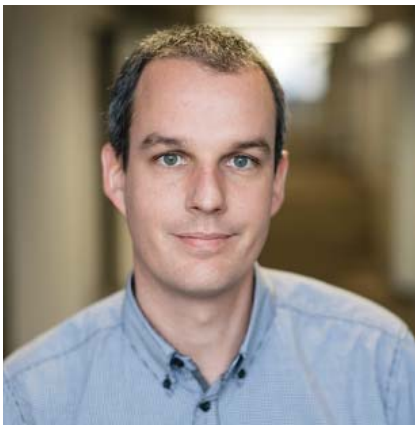
Helene Wehbe-Alause

Helene Wehbe-Alause has a PhD in Physics of semiconductors, on III-V quantum wells heterostructures for optical filtering, in collaboration with Schlumberger. After a few years in Thales avionics developing MEMS accelerometric and gyrometric sensors for space and aeronautics, she joined ST Microelectronics in 2000. Since 2011, she has been managing ST Process integration team for CIS : developing the BSI, 3D stacking brick, 90nm and 40nm SPAD technologies, and bringing in production CDTI based rolling and global shutters. In 2017 she also integrated the TCAD simulation team in her service in order that Simulation activities sustain the developments of new pixels from their conception until their full qualification. Since 2021, she has been appointed Director of the Technology for Optical Sensors Department which mission is supporting STM Imaging Division roadmap with developing differentiated technologies adapted to customer needs : provide innovating pixel architectures, from design to full validation of pixel performance, put in place and insure the quality and readiness for industrialisaton of the process flow for the technology.

Title: Advanced Optoelectronic Technologies : Device Optimization and Securing Production with Predictive Simulation Tool-chains

Abstract: The continuous evolution of semiconductor consumer electronic global market, including autonomous systems, augmented and virtual reality (AR/VR), and energy-efficient technologies, necessitates the development of advanced optical sensing solutions. These applications demand innovative optoelectronic devices, such as RGB and near-infrared (NIR) image sensors, but also time-of-flight optical sensors and multi-spectral ambient light sensing. Sequential 3D stacking, hybrid bonding and pixel size shrinkage has revolutionized CIS design, enabling differentiated pixel architectures that meet the demands of emerging applications and hold significant promise for the next generation of optical sensors. Metasurfaces, advanced optical filters and surface structuration technologies also further expands the capabilities of optical sensors, paving the way for high-resolution, energy efficient imaging and all-in-one sensing solutions. This paper presents a comprehensive overview of the recent state-of-the-art advancements in CMOS image sensors (CIS), emphasizing their technological breakthroughs, challenges, and future directions. We highlight the importance of predictive simulation tools to address these challenges and make the best integration of advanced CIS into complex systems. Advanced multi-physics simulation capabilities are required to model light propagation, carrier transport and material properties, but also for the integration of optical devices into larger system modules. Additionally, neural-network-based approaches are required to emulate and optimize large meta-surface optical systems, but also to make possible the optimization of new optical enablers such as meta-surface-based color routers.

Mathieu Luisier



Since 2022, Mathieu Luisier has been Full Professor of Computational Nanoelectronics at ETH Zurich, Switzerland. He graduated in electrical engineering in 2003 and received his PhD in 2007, both from ETH Zurich. During that time, he started the development of a state-of-the-art quantum transport simulator called OMEN. After a one-year post-doc at ETH, he joined in 2008 the Network for Computational Nanotechnology at Purdue University, USA, as a research assistant professor. In 2011 he returned to ETH Zurich to become Assistant and then Associate Professor. His current research interests focus on the modeling of nanoscale devices, such as advanced transistors based on classical semiconductors and 2-D materials, photo-detectors/emitters, and non-volatile resistive memory cells.

Title: Acceleration of atomistic NEGF: algorithms, parallelization, and machine learning

Abstract: The Non-equilibrium Green's function (NEGF) formalism is a particularly powerful method to simulate the quantum transport properties of nanoscale devices, e.g., transistors, photo-diodes, or memory cells, in the ballistic limit of transport or in the presence of various scattering sources such as electron-phonon, electron-photon, or even electron-electron interactions. The inclusion of all these mechanisms has been first demonstrated in small systems, composed of a few atoms, before being scaled up to larger structures made of thousands of atoms. Also the accuracy of the models has kept improving, from empirical to fully ab-initio ones. NEGF is nowadays widely used in combination with density functional theory (DFT) to investigate the electronic, thermal, or optical characteristics of different types of nano-devices. These progresses have been enabled by the development of dedicated numerical algorithms and by the parallelization of the workload, first on CPUs, now on GPUs.

In this presentation, I will review key achievements that have allowed to push back the limit of DFT+NEGF solvers beyond toy examples and I will illustrate them with recent applications. Also, I will show how graph neural networks and machine-learning can be leveraged to speed up ab-initio device simulations.

Lado Filipovic

Dr. Lado Filipovic is an Associate Professor and Director of the Christian Doppler Laboratory for Multi-Scale Process Modeling at TU Wien's Institute for Microelectronics. He earned his PhD in Microelectronics from TU Wien and specializes in semiconductor sensor technology and process simulations. His research focuses on integrated sensors, multi-scale process modeling, and novel semiconductor materials. He leads various projects on process simulations, equipment-informed inverse design, and novel material studies, working to advance semiconductor fabrication and device performance. His team has developed open-source TCAD tools like ViennaPS and ViennaEMC, widely used for process and device modeling. A Senior Member of IEEE, he collaborates with leading industry partners and academic institutions worldwide.

Title: From Atoms to Reactors: Multi-Scale Modeling for Semiconductor Fabrication

Abstract: Accurately predicting surface topography evolution during semiconductor processing is essential for advanced device manufacturing and Process/Design Technology Co-Optimization (PTCO/DTCO). PTCO bridges semiconductor process development and circuit design, ensuring that yield, performance, and manufacturability are optimized together. In this talk, we present multi-scale modeling approaches that span atomistic, feature, and reactor scales to enable predictive process design and optimization. At the atomic scale, first-principles methods such as DFT and molecular dynamics provide insight into fundamental surface reactions, including adsorption, desorption, and sputtering. These reactions define surface evolution models that are implemented at the feature scale using tools like ViennaPS, our open-source framework for simulating 3D topography evolution during etching and deposition. Chamber-scale plasma simulations provide spatially resolved ion and neutral flux distributions, ensuring that the surface evolution models are driven by realistic process conditions. To further improve model fidelity, experimental SEM/TEM images are used for automated calibration, allowing for the extraction and automated tuning of reaction rates and material-specific parameters. To improve efficiency, surrogate models of the plasma equipment can be integrated at the feature scale to capture reactor behavior without the cost of full-scale simulation. Finally, lithography-induced effects, such as non-uniform exposure and proximity effect corrections (PEC), are incorporated to account for variations in feature profiles introduced during patterning. This multi-scale approach allows for end-to-end simulation of semiconductor processes, supporting inverse design workflows and reducing reliance on costly experimental iteration. We demonstrate the capabilities required of today's process simulation frameworks through case studies involving FinFETs, 3D NAND, and photonic structures, highlighting how cross-scale modeling improves accuracy, efficiency, and scalability in technology development.

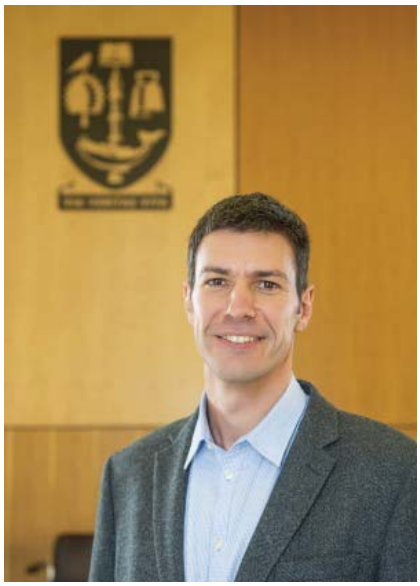
Andreas Rosskopf

Andreas Rosskopf studied Applied Mathematics with a focus on Numerical Simulation in Erlangen, Germany. Since 2012 he's with Fraunhofer IISB in Erlangen; in 2018 he founded the working group "AI-augmented Simulation " combing AI and numerical approaches for the simulation and optimization of power electronic devices and systems. Since 2023 he's head of the "Modeling and Artificial Intelligence" department of the Fraunhofer IISB designing digital solutions in the field of power electronics, Technology Computer-Aided Design and lithography.

Title: Scientific Machine Learning (SciML) - How the fusion of AI and physics is giving rise to promising simulation methodologies.

Abstract: Established approaches to simulating semiconductor processes and devices typically solve physically motivated equations or use Neural Networks (NN) trained with large amounts of measurement data to approximate the real system or process. With scientific machine learning (SciML), a new methodology is emerging that combines both and opens up new possibilities in taylored, real-time simulation and optimization of complex physical and chemical systems. We present and examine different NN architectures and learning strategies that allow approximating solutions of PDEs. We show the potential of separating model generation and inferance for (topology-)optimization, explainability and real-time simulation and provide an outlook on the possibilities of this method in future engineering processes.

Vihar Georgiev



Vihar is a Professor of Nanoelectronics and the Leader of the DeepNano Group at the University of Glasgow. He has more than 15 years of experience in developing numerical solvers and machine learning methods that are used for modelling and simulations of various semiconductor devices, such as nanowire transistors, tunnelling FETs, biosensors, current transport in inorganic molecules, Josephson's junctions, physical unclonable functions and molecular flash memories.
Vihar has participated in 12 European and UK projects in total. From 2018 until 2022 he held an EPSRC Industrial Fellowship called Quantum Simulator for Entangled Electronics. Since his appointment as a Lecturer in 2015, he has secured funding of around £1.5M as a PI and around £5.0M as a co-PI. For more information, please see his University of Glasgow.

Title: Modelling and simulations of biosensors: from analytical to machine learning approaches

Abstract: Biosensors can be broadly classified into different types based on the method used for signal transduction, including electrochemical, optical, thermal, piezoelectric and magnetic biosensors. Due to a vast area of possibilities, in this talk, I will focus my attention on electrochemical biosensors and I will discuss the underlying physical and electrical principles of operations and their areas of applications. Using simulations and modelling is the most cost, time and resource effective method to test new devices and explain physical, chemical and electrical concepts. To explain the operation of such electrochemical biosensor devices, I will present different simulations methods and approaches. This talk will cover various simulation techniques covering analytical and numerical methods and how these approaches are used to train neural networks. I will discuss the advantages and disadvantages of each of these methods and summarize the current state of the art in modelling of biosensors. I will use practical examples and case study emphasizing how hybrid modelling strategies can bridge the gap between physics-based and data-driven models.

Program

Wednesday, 24 of September

8:30–8:45	**Welcome to SISPAD 2025**	
8:45–9:45	**Emmanuel Leroux Dassault Systèmes** Plenary invited talk - Chair P. Blaise (Titane 2)	
9:45–10:00	**15 mins break**	
10:00–11:50	**Andreas Rosskopf (+4 talks)** Machine learning applications Titane 2	**Zlatan Stanojevic (+4 talks)** Advanced TCAD transport modeling Palladium 2
11:50–13:00	**Lunch**	
13:00–14:30	**Eric Guichard (+3 talks)** Emerging TCAD co-optimization methodologies Titane 2	**Vihar Georgiev (+3 talks)** Novel devices and sensors Palladium 2
14:30–14:50	**20 mins break**	
14:50–15:50	Quantum computing (3 talks) Titane 2	3D NAND Flash and DRAM (3 talks) Palladium 2
15:50–16:20	**30 mins break**	
16:20–16:35	**Sponsors presentations: LAM (Titane 2)** The name of the speaker has not been confirmed	
16:35–16:50	**Sponsors presentations: SYNOPSYS (Titane 2)** The name of the speaker has not been confirmed	
16:50–17:05	**Sponsors presentations: SILVACO (Titane 2)** The name of the speaker has not been confirmed	
17:05–17:20	**Sponsors presentations: LETI (Titane 2)** The name of the speaker has not been confirmed	
17:20–20:30	**Poster session and cocktail**	

Thursday, 25 of September

8:30–8:45	**Information on gala dinner**	
8:45–9:45	**Elisa Vianello CEA-Leti** Plenary invited talk - Chair D. Esseni (Titane 2)	
9:45–10:00	**15 mins break**	
10:00–11:50	**Helene Wehbe-Alause (+4 talks)** SPADs and photodiodes Titane 2	**Srinivas Raghvendra (+4 talks)** Power Devices Palladium 2
11:50–13:00	**Lunch**	
13:00–14:20	Methodologies for transport modeling (4 talks) Titane 2	Traps related modeling (4 talks) Palladium 2
14:20–14:30	**10 mins break**	
14:30–15:50	Process simulation : part 1 (4 talks) Titane 2	Full-band BTE and hopping transport (4 talks) Palladium 2
15:50–16:20	**30 mins break**	
16:20–17:40	Quantum transport in 2D devices (4 talks) Titane 2	Thermal simulation (3 talks) Palladium 2
19:00–22:00	**Gala dinner ("la Casemate" 2 Pl. Saint-Laurent, 38000 Grenoble)**	

Friday, 26 of September

8:30–8:45	**SISPAD 2026 announcement**	
8:45–9:45	**Tristan Meunier Quobly** Plenary invited talk - Chair D. Rideau (Titane 2)	
9:45–10:00	**15 mins break**	
10:00–11:50	**Mathieu Luisier (+4 talks)** Ab initio, machine learning, and quantum transport Titane 2	**Lado Filipovic (+4 talks)** Process simulation : part 2 Palladium 2
11:50–12:00	**Closing remarks**	
12:00–13:00	**Lunch**	

List of talks

Plenary invited talks

8:45-9:45

Virtual Twins for Semiconductor Design and Manufacturing Processes
Emmanuel Leroux[1]
[1] Dassault Systèmes
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8:45-9:45

Resistive memories: multifaced impact on neuromorphic computing
Elisa Vianello[1]
[1] CEA-Leti
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8:45-9:45

Transport characterization and quantum dot coupling in commercial 22FDX®
Tristan Meunier[1]
[1] Quobly
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Machine learning applications

Chair : Andreas Rosskopf (Fraunhofer IISB) & Co-chair : Denis Rideau (STMicroelectronics)

Invited Talk

10:00-10:30

Scientific Machine Learning (SciML) - How the fusion of AI and physics is giving rise to promising simulation methodologies
Andreas Rosskopf[1]
[1] Fraunhofer IISB
Page 59

Talks

10:30-10:50

A Novel CNN-Based BEOL Contour Modeling Solution for Parasitic R/C Extraction
Chang-Hung Yu[1], *Jim Liang*, *Gary Lee*, *Chao-Te Lee*, *Wei-Pin Luo*, *Ke-Wei Su*, *Kuan-Lun Cheng*, *Chung-Kai Lin*
[1] TSMC
Page 63

10:50-11:10

Modeling Nickel-Silicidation using Physics-Informed Machine Learning
Christopher Straub[1], *Simon Mundinar*, *Andreas Rosskopf*
[1] Fraunhofer IISB
Page 67

11:10-11:30

Inverse design of optical metasurface for CMOS imagers: a multi-objective optimization approach
Damien Maitre[1], *Denis Rideau*, *Olivier Jeannin*, *Clémence Jamin-Mornet*, *Charly Leblanc*, *Maxime Darnon*, *Raphaël Clerc*, *Jean-Philippe Banon*, *Coumba Gaye*, *Fatima Omeis*, *Louis-Henri Fernandez-Mouron*, *Loumi Tremas*, *Mathys Le Grand*, *Adam Fuchs*, *Pascal Urard*, *James Downing*, *Bruce Rae*
[1] STMicroelectronics
Page 71

11:30-10:50

Process-Performance Variability Modeling of Inner Spacer Etch in GAA FETs
Om Maheshwari[1], *Nihar Mohapatra*
[1] Indian Institute of Technology Gandhinagar
Page 75

Advanced TCAD transport modeling

Chair : Zlatan Stanojevic (GTS) & Co-chair : François Triozon (CEA-LETI)

Invited Talk

10:00-10:30

Is there anything left to do in TCAD?
Zlatan Stanojevic[1]
[1] GlobalTCAD
Page 79

Talks

10:30-10:50

Stabilization of the Drift-Diffusion Model for Arbitrary Carrier Statistics
Max Renner[1], *Tobias Linn*, *Christoph Jungemann*
[1] RWTH Aachen University
Page 83

10:50-11:10

Predictive Nanoscale Simulations for THz Regime
Ulrik G. Vej-Hansen[1], *Kevin Galiano*, *Nelson de Almeida Braga*, *Tony Riccobono*, *Thomas J. Knight*, *Ricardo Borges*
[1] Synopsys
Page 87

11:10-11:30

An Effective-Medium TCAD Model of Amorphous In-Ga-Zn-O (a-IGZO) Suitable For Large-Area Devices
Mischa Thesberg[1], *Zlatan Stanojevic*, *Franz Schanovsky*, *José-Maria Gonzalez-Medina*, *Gerhard Rzepa*, *Ferdinand Mitterbauer*, *Oskar Baumgartner*, *Markus Karner*
[1] Global TCAD Solutions GmbH (GTS)
Page 91

11:30-11:50

Accurate Carrier Dynamics for a Kane Dispersion Relation
Josef Gull[1]
[1] Institute for Microelectronics, TU Vienna
Page 95

Emerging TCAD co-optimization methodologies

Chair : Eric Guichard (SILVACO) & Co-chair : Helene Jacquinot (CEA-LETI)

Invited Talk

13:00-13:30

Driving Four Decades of TCAD Innovation: From Physical Simulation to AI-Powered Digital Twins
Eric Guichard[1]
[1] Silvaco
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Talks

13:30-13:50

Novel Block-Level DTCO Solution for Advanced Logic Technology Path-Finding
Eun Bi Nam[1], *Takeshi Okagaki*, *Jeesoo Chang*, *Yong Seok Song*, *Seunghyun Song*, *Yang Lu*, *Hong Hyun Park*, *Yonghee Park*, *Dae Sin Kim*
[1] Samsung Electronics
Page 103

13:50-14:10

A New Module for Automated Optimization of Process TCAD Model Parameters
Roman Kostal[1], *Tobias Reiter*, *Lado Filipovic*
[1] Institute for Microelectronics, TU Vienna
Page 107

14:10-14:30

Performance Evaluation of Low Temperature Source/Drain Epitaxy Process Targeting Contact Resistance Scaling for Advanced Gate-All-Around Technology
Pratik B. Vyas[1], *Lars P. Tatum*, *Ning Yang*, *Ashish Pal*, *Nicolas Breil*, *Benjamin Colombeau*, *El Mehdi Bazizi*
[1] Applied Materials Inc.
Page 111

Novel devices and sensors

Chair : Vihar Georgiev (University of Glasgow) & Co-chair : Sébastien Martinie (CEA-LETI)

Invited Talk

13:00-13:30

Machine learning enhanced device and material simulations of various electronic devices
Vihar Georgiev[1]
[1] University of Glasgow
Page 115

Talks

13:30-13:50

Modeling and investigation of auto focus disparity sensitivity for CMOS image sensors with sub-micrometer scale pixel size
Euiyoung Song[1], *Jae Ho Kim*, *Kwanghee Lee*, *Jongsu Yoon*, *Sungchul Kim*, *Seunghyun Hong*, *Sung-Su Kim*, *Yonghee Park*, *Dae Sin Kim*
[1] Samsung Electronics
Page 119

13:50-14:10

Modeling SOT-Driven Domain Wall Motion in MTJ Switching.
Trisha Bhowmik[1], *Yang Xiang*, *Maxwel Gama Monteiro*, *Siddharth Rao*, *Fernando Garcia Redondo*, *Jan Van Houdt*, *Kristiaan Temst*
[1] IMEC
Page 123

14:10-14:30

TCAD Analysis on the Geometry Effects in Three-Independent-Gates Reconfigurable FETs
Jose Maria Gonzalez-Medina[1], *Lee-Chi Hung*, *Yuxuan He*, *Amine Arsalani*, *Oskar Baumgartner*, *Thomas Mikolajick*, *Jens Trommer*, *Chhandak Mukherjee*, *Markus Karner*
[1] Global TCAD Solutions GmbH
Page 127

Quantum computing

Chair : Biel MARTINEZ I DIAZ (CEA-LETI) & Co-chair : François Triozon (CEA-LETI)

Talks

14:50-15:10

Multi-scale simulation framework for the modelling of charge capture and emission in spin qubit devices

Gabriele Boschetto[1], *Christoph Wilhelmer*, *Lukas Cvitkovich*, *Jing Li*, *Dominic Waldhoer*, *Tibor Grasser*, *Biel Martinez i Diaz*

[1] CEA-Leti

Page 131

15:10-15:30

Simulating two-qubit gates under the influence of charge defects in an FD-SOI device

Pericles Philippopoulos[1], *Félix Beaudoin*, *Philippe Galy*

[1] Nanoacademic Technologies Inc.

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15:30-15:50

Quantum Algorithms for Simulating Quantum Transport via the Time-Dependent Open-System Schrödinger Equation

Satofumi Souma[1]

[1] Kobe University

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3D NAND Flash and DRAM

Chair : Markus Karner (GTS) & Co-chair : Sébastien Martinie (CEA-LETI)

Talks

14:50-15:10

Airgap-induced Field Enhancement to Improve Memory Operation in 3-D NAND Flash Memory
Devin Verreck[1], *Sana Rachidi*, *Geert Van den bosch*, *Maarten Rosmeulen*
[1] imec
Page 143

15:10-15:30

Data science statistical approach to percolative conduction in poly-Si based 3D NAND channels
Aurelio Giancarlo Mauri[1], *Marco Vezzoli*, *Luca Chiavarone*, *Sebastiano Baggi*, *David Refaldi*, *Spinelli Alessandro*, *Christian Monzio Compagnoni*
[1] Micron Technology and Development
Page 147

15:30-15:50

Understanding the Floating-Body Effect Simulation and Optimization in 3D-DRAMs
Salvatore Maria Amoroso[1], *Geert Eneman*, *Plamen Asenov*, *Meng-Hsuan Ke*, *Nouredine Rassoul*, *Inhee Lee*, *Attilio Belmonte*, *Ko-Hsin Lee*, *Xi-Wei Lin*, *Victor Moroz*
[1] Synopsys
Page 151

SPADs and photodiodes

Chair : Helene Wehbe-Alause (STmicroelectronics) & Co-chair : Joris Lacord (CEA-LETI)

Invited Talk

10:00-10:30

Device Optimization and Securing Production with Predictive Simulation Tool-chains
Helene Wehbe-Alause[1]
[1] STMicroelectronics
Page 155

Talks

10:30-10:50

Statistical SPAD Compact Model Dedicated to Pixel Transients Simulations
Jean-Robert Manouvrier[1], *Denis Rideau*, *Gilles Gouget*, *Mohammed Al-Rawhani*, *Elsa Lacombe*, *Isobel Nicholson*, *Marie BASSET*, *Bastien Mamdy*, *Raul-andres Bianchi*, *Sara Pellegrini*
[1] STMicroelectronics
Page 159

10:50-11:10

Hole-Induced Avalanche and its Role in Dark Current in SPADs
Isobel Nicholson[1], *Gabriel Mugny*, *Remi Helleboid*, *Bastien Mamdy*, *Dominique Golanski*, *Sebastien Place*, *Patryk Maciakez*, *Denis Rideau*
[1] ST Microelectronics
Page 163

11:10-11:30

Physical-based model for the optical simulation of III-V photodiodes
Gabriel Mugny[1], *Denis Rideau*, *Jules Tillement*, *Weronika Letka*, *Pascal Fonteneau*
[1] STMicroelectronics
Page 167

11:30-11:50

Improved stochastic SPAD quenching model including build-up field effect
Rémi HELLEBOID[1], *Samuel Dahan*, *Kenzo Morel-Handa*, *Gabriel Mugny*, *Isobel Nicholson*, *Denis Rideau*, *Marco Pala*, *Philippe Dolffus*, *Jérôme Saint-Martin*
[1] Université Paris Saclay
Page 171

Power devices

Chair : Srinivas Raghvendra (SYNOPSYS) & Co-chair : Rihab Chouk (CEA-LETI)

Invited Talk

10:00-10:30

Advances in Power Electronics Design Fueled by Hyperconvergence
Srinivas Raghvendra[1]
[1] SYNOPSYS
Page 175

Talks

10:30-10:50

Development of a Gaussian Approximation Potential for GaN with Point Defects and Mg Impurities
Yuki Ohuchi[1], *Robert Stella*, *Lado Filipovic*
[1] Institute for Microelectronics, TU Wien
Page 179

10:50-11:10

Artificial Intelligence Driven Optimization of 1200V SiC DMOS
David Green, *Thomas Jokinen*, *Stefania Carapezzi*[1]
[1] Silvaco
Page 183

11:10-11:30

3D Wide-Area TCAD Approach to Address Avalanche Breakdown in IGBT Edge Termination
Massimiliano Galvagno[1], *Lucia Zullino*, *Simone Dario Mariani*, *Paola Zuliani*, *Salvatore-Fabio Liotta*, *Silvia Cannizzaro*, *Gerardo Malavena*, *Christian Monzio Compagnoni*, *Alessandro Sottocornola Spinelli*
[1] Politecnico di Milano
Page 187

11:30-11:50

Modeling of hole generation process in AlGaN/GaN HEMTs
Ying-Chun Kuo[1], *Hao Yu*, *Nelson Almeida de Braga*, *Jingtian Fang*, *Amratansh Gupta*, *Sachin Yadav*, *AliReza Alian*, *Uthayasankaran Peralagu*, *Nadine Collaert*, *Bertrand Parvais*
[1] imec
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Traps related modeling

Chair : Salvatore Amoroso (SYNOPSYS) & Co-chair : Benoit Sklénard (CEA-LETI)

Talks

13:00-13:20

Modeling of PMOS Off-State Stress by introducing an energy resonant cross-section into the energy-driven hot carrier degradation model
Hyunjae Kim[1]
[1] Samsung Electronics
Page 195

13:20-13:40

Composition Effect of Tunneling and Charge Trap Layer for Enhanced Cycle Retention in VNAND Flash Memory
Hyeyoung Kwon[1]
[1] samsung electronics company
Page 199

13:40-14:00

Unveiling fast interface trap dynamics in monolayer MoS2 FETs
Rittik Ghosh[1], *Alexandros Provias*, *Alexander Karl*, *Rajarshi Roy Chaudhuri*, *Dominic Waldhör*, *Theresia Knobloch*, *Christoph Wilhelmer*, *Tibor Grasser*
[1] Institute for Microelectronics, TU Wien
Page 203

14:00-14:20

Modeling and Analysis of Electron Trapping Mechanisms in Al2O3/Si3N4 and Al2O3/Si3N4/SiO2 Charge Trap Devices
Joonhyung Cho[1], *Joon Hwang*, *Suyoung Park*, *Min-Kyu Park*, *Jong-Ho Lee*
[1] Seoul National University
Page 207

Methodologies for transport modeling

Chair : Hideki Minari (SONY) & Co-chair : François Triozon (CEA-LETI)

Talks

13:00-13:20

Deterministic Boltzmann Transport Equation Solver: Validation and Heat Generation Modeling
Ying-Lun Kao[1], *Christoph Jungemann*, *Michel Houssa*, *Stanislav Tyaginov*
[1] imec
Page 211

13:20-13:40

Efficient and Accurate Full Band Semi-Classical Monte-Carlo Transport Simulation Using Smearing Method and Marching Tetrahedra Algorithm
Donghyeok Lee[1], *Seong Woo Kang*, *Leonard Register*, *Sanjay Banerjee*, *Jiwon Chang*
[1] Department of Materials Science and Engineering, Yonsei University
Page 215

13:40-14:00

Analysis of Transient Quantum Transport in Nanoscale Devices Using Density Matrix Methods
Mathias Pech[1], *Jonas Neu*, *Dirk Schulz*
[1] TU Dortmund
Page 219

14:00-14:20

Quantum limit of the contact resistance to low-dimensional materials
Emeric Deylgat[1], *Bart Sorée*, *William Vandenberghe*
[1] The University of Texas at Dallas
Page 223

Process simulation (1)

Chair : Lado Filipovic (TU Wien) & Co-chair : Olga Cueto (CEA-LETI)

Talks

14:30-14:50

Purge Effect Simulation of Atomic Layer Deposition for High Aspect Ratio Structure
Satoshi Nakamura[1], *Hisashi Kotakemori*, *Kenta Yashima*, *Taishi Ikeda*, *Takumi Ohmura*, *Yasuyuki Kayama*, *YunTae Lee*, *Gwangsu Yoo*, *Yukihide Tsuji*, *Shinwook Yi*, *Jaehoon Jeong*, *Dae Sin Kim*
[1] Samsung Japan Corporation
Page 227

14:50-15:10

Physics-Based Multi-Scale Modeling of Angled Reactive Ion Etching
Robert Stella[1], *Sabine Leroch*, *Tobias Reiter*, *Andreas Hössinger*, *Lado Filipovic*
[1] CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors at the Institute for Microelectronics, TU Wien
Page 231

15:10-15:30

Simulation of a Polymer-Free DRIE Process Using SF6/O2 Plasma Etching
Tobias Reiter[1], *Alexander Toifl*, *Andreas Hössinger*, *Lado Filipovic*
[1] CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors, Institute for Microelectronics, TU Wien
Page 235

15:30-15:50

Modeling on Tilting and Twisting Distortions of 3D NAND High-Aspect-Ratio Etching
Yuxuan Zhai[1], *Junjie Li*, *Rui Chen*, *Ling Li*
[1] Institute of Microelectronics, Chinese Academy of Sciences
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Full-band BTE and hopping transport

Chair : Kai Tak Lam (TSMC) & Co-chair : Philippe Blaise (SILVACO)

Talks

14:30-14:50

Multiscale Modeling of High-Field Transport in 4H-SiC: A Novel Avalanche Generation Model Based on Full Band Monte Carlo Simulation
Mitsuhiro Sengoku[1], *Souzou Kanie*
[1] Toshiba Electronic Devices Storage Corporation
Page 243

14:50-15:10

Anisotropic electron polaron mobility in V2O5: from ab initio to Kinetic Monte Carlo
Hala Houmsi[1], *Benoit Sklénard*, *François Triozon*, *Marc Guillaumont*, *Jing Li*
[1] Lynred
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15:10-15:30

Analyzing full band transport in 2D TMDs using the Monte Carlo method
Nils Vansteenvoort[1], *Gautam Gaddemane*, *Maarten Van de Put*, *Bart Sorée*
[1] Imec
Page 251

15:30-15:50

Full Band Semi-Classical Monte-Carlo Simulation of Layer Number-Dependent Electron Transport in MoS2 and InSe
Sukhyeong Youn[1], *Donghyeok Lee*, *Jiwon Chang*
[1] Yonsei University
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Quantum transport in 2D devices

Chair : Daniel Lizzit (university of udine) & Co-chair : François Triozon (CEA-LETI)

Talks

16:20-16:40

Layer and Stacking Effects on Transport Properties in Steep-Slope Cold-Metal-Source FETs
Chiao-Yu Chang[1], *Bart Sorée*, *Aryan Afzalian*
[1] Imec, Kapeldreef 75, 3001 Leuven, Belgium Page 259

16:40-17:00

Ab-initio-NEGF Fundamental Roadmap for Carbon-Nanotube and Two-Dimensional-Material MOSFETs at the Scaling and VDD Limit
Aryan Afzalian[1]
[1] imec Page 263

17:00-17:20

Ab-initio transport study of Source-to-Channel Resistance in Metal-MoS2 Top Contacts including Image Force Barrier Lowering in a Heterogeneous Dielectric Environment
Alessandro Pilotto[1], *Daniel Lizzit*, *Marco Pala*, *David Esseni*
[1] University of Udine Page 267

17:20-17:40

Multi-band model Hamiltonian for tunnel devices with van der Waals heterojunctions
Owen Loison[1], *Adel M'Foukh*, *Davide Romanin*, *Marco Pala*, *Philippe Dollfus*
[1] C2N Page 271

Thermal simulation

Chair : Vincent Mandrillon (CEA-LETI) & Co-chair : Sébastien Martinie (CEA-LETI)

Talks

16:20-16:40

Thermal Resistance Decomposition of Packaging Solutions in Advanced CMOS Nodes
Oscar Restrepo[1], *Steve Ludvik*, *Jason Lestage*, *Oscar Gonzalez*, *William Taylor*, *purushothaman srinivasan*
[1] GLOBALFOUNDRIES
Page 275

16:40-17:00

Device-to-Package Level Thermal Risk Analysis of the Back-Side Power Delivery Network
Dongun Shin[1], *Jae Hee Choi*, *Takeshi Okagaki*, *Jeesoo Chang*, *Eun Bi Nam*, *Jinkyu Kim*, *Hidenobu Fukutome*, *Hyeongsub Song*, *SungJoon Park*, *Yonghee Park*, *Keun Hwi Cho*, *Sungjae Lee*, *Dae Sin Kim*
[1] Samsung Electronics
Page 279

17:00-17:20

Self-Heating Coupled Hot Carrier Degradation in Stacked GAA FETs Based on Full Quantum Simulation Framework
Hongwei Zhou[1], *Haoran Wang*, *Zirui Wang*, *Zixuan Sun*, *Runsheng Wang*, *Lang Zeng*
[1] Beihang university
Page 283

Ab initio, machine learning, and quantum transport

Chair : Mathieu Luisier (ETH Zurich) & Co-chair : François Triozon (CEA-LETI)

Invited Talk

10:00-10:30

Acceleration of atomistic NEGF: algorithms, parallelization, and machine learning
Mathieu Luisier[1]
[1] ETH Zurich
Page 287

Talks

10:30-10:50

Machine-Learned Hamiltonians for Quantum Transport Simulation of Valence Change Memory
Chen Hao Xia[1], *Manasa Kaniselvan*, *Marko Mladenovic*, *Mathieu Luisier*
[1] ETH Zürich
Page 291

10:50-11:10

Efficient Quantum-Mechanics-Based Molecular Dynamics Through Machine Learning-Driven Density Functional Theory Hamiltonian
Guenseok Choi[1], *Mincheol Shin*
[1] kaist
Page 295

11:10-11:30

Solving the Bethe-Salpeter Equation in the NEGF formalism
Jiang Cao[1], *Nicolas Vetsch*, *Vincent Maillou*, *Anders Winka*, *Alexander Maeder*, *Alexandros Nikolaos Ziogas*, *Mathieu Luisier*
[1] ETH Zurich
Page 299

11:30-11:50

Mechanisms of HfSe2 layer-by-layer oxidation and clean van der Waals interface formation with 2D semiconductors: First-principles molecular dynamics simulation study
Joonho Park[1], *Yong-Hoon Kim*
[1] Korea Advanced Institution of Science and Technology
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Process simulation (2)

Chair : Lado Filipovic (TU Wien) & Co-chair : Olga Cueto (CEA-LETI)

Invited Talk

10:00-10:30

From Atoms to Reactors: Multi-Scale Modeling for Semiconductor Fabrication
Lado Filipovic[1]
[1] TU Wien
Page 307

Talks

10:30-10:50

High-Fidelity and Efficient Epitaxial Growth Simulations via Hybrid Meshing and BVH-based Ray Tracing
Hiroyuki Kubotera[1], *Chihak Ahn*, *Byounghak Lee*, *Marton Voeroes*, *Woosung Choi*, *Anthony Payet*, *Alexander Schmidt*, *Geunsang Yoo*, *Dae Sin Kim*
[1] Samsung Semiconductor Inc.
Page 311

10:50-11:10

Full device scale atomistic kinetic lattice Monte-Carlo simulation of metal-induced lateral crystallization process
Jun Jung[1], *Alexander Schmidt*, *Byounghak Lee*, *Woosung Choi*, *Joohyun Jeon*, *Seungmin Lee*, *Dae Sin Kim*
[1] Samsung Electronics
Page 315

11:10-11:30

From CMP Surface Prediction to Defect Detection: An AI-Driven Virtual Metrology-TCAD Framework
Yeji Kim[1], *Min-Chul Park*, *Sangyeon Kim*, *Usuk Chae*, *Byungchul Shin*, *Segab Kwon*, *SeongRyeol Kim*, *Yoon-Suk Kim*, *Jae-Hyun Kang*, *Young-Gu Kim*, *Joong-Won Jeon*, *Dae Sin Kim*
[1] Samsung Electronics
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Atomic-Level Monte Carlo Modeling of SiN Deposition by PECVD
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