

## Conference venue

MINATEC Conference Center, 3 Parvis Louis Néel, 38054 Grenoble, FRANCE.

## Important dates (planned)

Two-pages abstract*	April 8, 2025
Notification of acceptance	May 27, 2025
Extended 4-pages final paper*	June 24, 2025
Early registration	July 15, 2025
Late registration	August 19, 2025

\*Submissions should be made through the website: https://sispad2025.inviteo.fr/

## **Organizing Committee**

J-C. Barbé (CEA-Leti, chair), D. Rideau (STMicroelectronics, co-chair); S. Martinie (CEA-Leti, TPC chair), B. Rae (STMicroelectronics, TPC co-chair);

P. Blaise (SILVACO, workshop chair), F. Triozon (CEA-Leti, workshop co-chair);

S. Barbier (CEA-Leti, local org.).

## Technical areas

- Modeling and simulation of all types of semiconductor devices, including FinFETs, GAA FETs, ultra-thin SOI devices, emerging memory devices, new material-based nanodevices, optoelectronic devices, TFTs, sensors, power electronic devices, spintronic devices, tunnel FETs, SETs, organic electronic devices, and bioelectronic devices;
- Modeling and simulation of all sorts of semiconductor processes, including first principles material design, and growth simulation of nano-
- Fundamental aspects of device modeling and simulation, including quantum transport, thermal transport, fluctuation, noise, and reliability;
- Compact modeling for circuit simulation, including low-power, high frequency, and power electronics applications;
- Process/device/circuit co-simulation in context with system design and verification;
- Equipment, topography, lithography modeling;
- Interconnect modeling, including noise and parasitic effects;
- Numerical methods and algorithms, including grid generation, userinterface, and visualization;
- Metrology for the modeling of semiconductor devices and processes;
- Multiscale approach from First Principles to TCAD simulations;
- Artificial intelligence, Neural Network, Differentiable programming;
- Neuromorphic devices and quantum computing;
- ✓ Multi-physics simulation.









